CLAIMS

We claim:

1. Apparatus embedded in a processor system comprising:

an auxiliary instruction queue (IQ) including a plurality of storage registers programmable with a set of instructions; and

control means for governing the programming of said auxiliary IQ with said set of instructions and for controlling insertion of said programmed instructions of said auxiliary IQ into an instruction execution stream of said processor system substantially without interrupting processing operations thereof.

2. The apparatus of claim 1 wherein the auxiliary IQ includes means responsive to an execution signal for accessing programmed instructions from the auxiliary IQ in a predetermined order for insertion into the instruction execution stream of the processor system.

3. The apparatus of claim 2 wherein the accessing means accesses the instructions from the auxiliary IQ in an addressable sequential order.

4. The apparatus of claim 2 wherein the accessing means accesses the instructions from the auxiliary IQ automatically in response to the execution signal.

5. The apparatus of claim 2 wherein the accessing means accesses the instructions from the auxiliary IQ at a rate commensurate with a processor system clock..

6. The apparatus of claim 2 wherein the control means includes means for gating the instructions accessed from the auxiliary IQ into an instruction pipeline of the processor system for execution by the processor system.

7. The apparatus of claim 2 wherein the auxiliary IQ includes a designated register programmable to characterize the set of instructions programmed therein; and wherein the accessing means is governed by the characterization of said designated register.

8. The apparatus of claim 1 wherein the control means includes means for controlling the operation of a program counter of the processor system during the insertion of the

programmed instructions of the auxiliary IQ into the instruction execution stream of the processor system.

9. The apparatus of claim 1 including a host interface means; and wherein the auxiliary IQ includes means for receiving instructions to be programmed therein from an external host device through said host interface means.

10. The apparatus of claim 9 wherein the instructions are received from the host device through the host interface means and programmed into the auxiliary IQ without interrupting the processing operations of the processor system.

11. The apparatus of claim 9 wherein the host interface means comprises a JTAG interface including serial scan chains coupled to the instruction queue.

12. The apparatus of claim 9 wherein the host interface means comprises a host peripheral interface.

13. The apparatus of claim 12 wherein the host peripheral interface is selected from the group comprising a serial peripheral interface and a parallel peripheral interface.

14. The apparatus of claim 9 wherein the instructions received from the host device comprise debug instructions.

15. The apparatus of claim 14 wherein the control means includes storage registers for temporarily storing data for and resulting from the execution of the debug instructions; and wherein the control means includes means for controlling the transfer of data between said storage registers and the host device through the host interface means without interrupting the processing operations of the processor system.

16. The apparatus of claim 9 wherein the instructions received from the host device comprise instructions for transferring data between the host device and the processor system.

17. The apparatus of claim 16 wherein the control means includes storage registers for temporarily storing data for and resulting from the execution of the data transfer instructions; and wherein the control means includes means for controlling the transfer of data between said storage registers and the host device through the host interface means without interrupting the processing operations of the processor system.

18. The apparatus of claim 1 wherein the auxiliary IQ is memory mapped as part of a memory space of the processor system; and wherein the auxiliary IQ is coupled to a bus of the processor system for being programmed with instructions from the processor system.

19. The apparatus of claim 18 wherein the instructions received from the processor system comprise debug instructions.

20. The apparatus of claim 18 wherein the instructions received from the processor system comprise a serial boot loader.

21. The apparatus of claim 1 wherein the auxiliary IQ is memory mapped as part of a memory space of the processor system; and wherein the auxiliary IQ is coupled to a bus of the processor system for being programmed with data from the processor system.

22. The apparatus of claim 1 wherein the control means includes means for configuring said apparatus into a plurality of operational modes.

23. The apparatus of claim 1 wherein the control means includes at least one event state detector for triggering the insertion of the programmed instructions of said auxiliary IQ into the instruction execution stream of the processor system.

24. The apparatus of claim 23 wherein the control means is coupled to a bus of the processor system; and wherein the at least one event state detector comprises a breakpoint detector.

25. The apparatus of claim 23 wherein the control means is coupled to a bus of the processor system; and wherein the at least one event state detector comprises a watchpoint detector.

26. Debug apparatus embedded in a processor system that has a debug monitor program stored in a program memory thereof, said apparatus comprising:

an auxiliary instruction queue (IQ) including a plurality of storage registers programmable with a set of debug instructions, said auxiliary IQ being coupled to a bus of the processor system, said storage registers being memory mapped to render the auxiliary IQ part of the memory space of the processor system; and

control means for governing the programming of said auxiliary IQ with said set of debug instructions accessed from the debug monitor program over said bus and for controlling insertion of said programmed debug instructions of said auxiliary IQ into an instruction execution stream of said processor system substantially without interrupting processing operations thereof.

27. The debug apparatus of claim 26 including a communication interface for coupling the control means with a host system external the processor system for directing the operations of the control means through commands from the host system.

28. The debug apparatus of claim 27 wherein the control means includes storage registers for temporarily storing data for and resulting from the execution of the debug instructions; and wherein the control means includes means for controlling the transfer of data between said storage registers and the host system through the communication interface without interrupting the processing operations of the processor system.

29. The debug apparatus of claim 26 wherein the control means includes at least one event state detector for triggering the insertion of the programmed debug instructions of said auxiliary IQ into the instruction execution stream of the processor system.

30. The debug apparatus of claim 26 wherein the control means includes storage registers for temporarily storing data for and resulting from the execution of the debug instructions.

31. Protection apparatus embedded in an integrated circuit (IC) processor system comprising:

an auxiliary data queue (DQ) including a plurality of storage registers for temporary storage of data, each said storage register being fabricated in the IC to survive an upset transient, said auxiliary DQ being coupled to a bus of the processor system, said storage registers being memory mapped to render the auxiliary DQ part of the memory space of the processor system; and

monitor means for detecting an onset of the upset transient; and

control means governed by said monitor means for transferring data of selected registers of the processor system into registers of said auxiliary DQ for storage during said upset transient.

32. The protection apparatus of claim 31 wherein the data comprises instructions of at least one program.

33. The protection apparatus of claim 32 wherein control means is governed by said monitor means for program operation during said upset transient.

34. The protection apparatus of claim 31 wherein the upset transient comprises a high radiation upset transient.

35. The protection apparatus of claim 31 wherein the auxiliary DQ comprises majority voted registers; and including means for powering down systems external to the IC processor during the upset transient.

36. The protection system of claim 35 wherein the monitor means includes means for detecting an end of the upset transient; wherein the powering means includes means for restoring power to the external systems when said end is detected; and wherein the control means includes means for transferring data stored in the registers of the auxiliary DQ during the upset transient back to their corresponding processor system registers upon restoration of power.

37. The protection system of claim 31 wherein the monitor means includes means for detecting an end of the upset transient; and wherein the control means includes means for transferring data stored in the registers of the auxiliary DQ during the upset transient back to their corresponding processor system registers upon detection of said end.

38. The protection apparatus of claim 31 wherein the data of the selected registers of the processor system represent a state thereof at the onset of the upset transient.

39. The protection apparatus of claim 31 wherein the auxiliary DQ is programmable with instruction sequences and operable to insert said programmed instruction sequences into an instruction execution stream of the processor system.

40. Method of protecting an integrated circuit (IC) processor system against an upset transient comprising the steps of:

detecting an onset of the upset transient;

transferring data of selected registers of the processor system into upset transient survivable registers of an auxiliary data queue (DQ) upon said detected onset; and

storing said data in said registers of the auxiliary DQ during the upset transient.

41. The method of claim 40 wherein the upset transient comprises a high radiation upset transient.

42. The method of claim 40 wherein the data of the selected registers is transferred to majority voted registers of the auxiliary DQ; and including the step of powering down systems to the IC processor during the upset transient.

43. The method of claim 42 including the steps of detecting an end of the upset transient; restoring power to the processor when said end is detected; and transferring data stored in the registers of the auxiliary DQ during the upset transient back to their corresponding processor system registers upon restoration of power.

44. The method of claim 40 including the steps of detecting an end of the upset transient; and transferring data stored in the registers of the auxiliary DQ during the upset transient back to their corresponding processor system registers upon detection of said end.

45. The method of claim 40 wherein the data of the selected registers of the processor system transferred to the auxiliary DQ represent a state thereof at the onset of the upset transient.

46. The method of claim 40 including the steps of programming the registers of the auxiliary DQ with instruction sequences; and operating the auxiliary DQ to insert said programmed instruction sequences into an instruction execution stream of the processor system.

47. Auxiliary boot loader apparatus embedded in a processor system and operable in a power-up mode of said processor system, said apparatus comprising:

an auxiliary instruction queue (IQ) including a plurality of storage registers configurable in said power-up mode to store a set of boot loader instructions, said registers of the auxiliary IQ being accessible by the processor system; and

means for detecting said power-up mode and causing said processor system to access and execute the stored instructions of said auxiliary IQ.

48. The apparatus of claim 47 including a cache operable as a memory of the processor system during said power-up mode; and a communication interface; and wherein the processor system is operable to execute the boot loader instructions of the auxiliary IQ to cause a stream of instructions to be loaded into the cache from an external system through the communication interface.

49. The apparatus of claim 48 including means for causing the execution of the instructions loaded into the cache.

50. The apparatus of claim 47 wherein the auxiliary IQ is reconfigurable to another mode of operation.